AN3168
Application note

Non-insulated SCR / Triac control circuits

Introduction

In alternating current applications the direct current power supply for low-voltage electronic devices (MCU, LEDs, optocouplers, Triacs and so on) can be provided using one of several different circuits. There are traditionally two major types of power supplies used in appliances, capacitive power supply and linear power supply using a step-down transformer. Today, designers are using more and more switches mode power supplies (SMPS) to achieve higher output current levels and especially lower standby power consumption. The power supply choice is a trade-off between several parameters. These are the cost, the required power, the output voltage level and polarity, the standby power consumption and the necessity or not of an electrical insulation between the mains and the low output DC voltage.

This application note considers only non-insulated power supplies. After a brief description of the triggering quadrants and key parameters for SCR, Triac, ACS and ACST, the usual control circuits are described according to the output voltage polarity of the power supply. Finally, some examples of negative power supply circuits are introduced.

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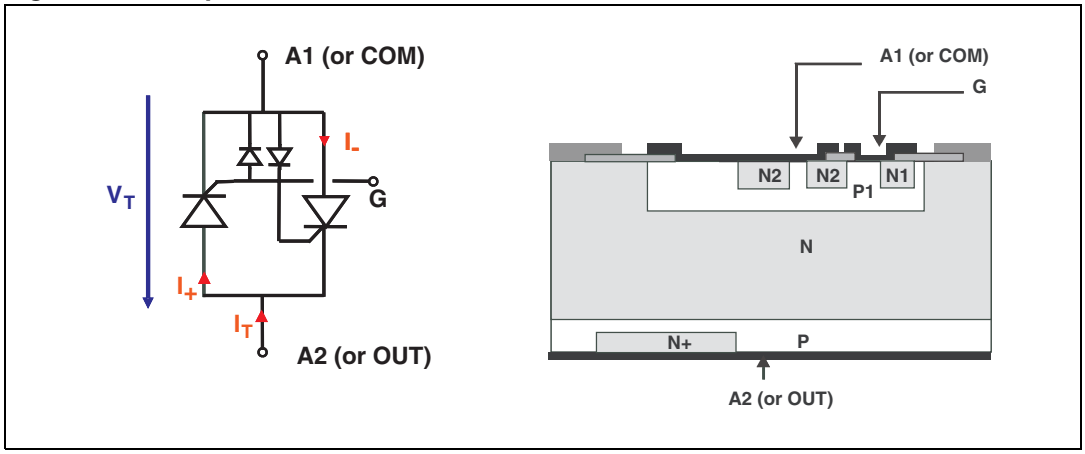
1 Triggering quadrants and key parameters

To switch-on an SCR, Triac, ACS or ACST, a gate current must be applied on its gate pin (G). The gate current flows between Gate (G) and Cathode (K) for SCR, or between Gate and terminal A1 for Triac, or between Gate and terminal COM for ACS and ACST.

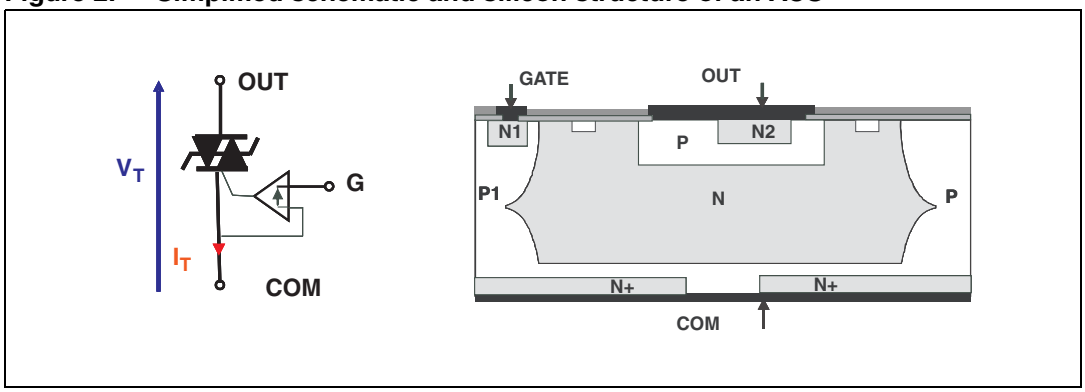
For Triac and ACST, the gate current could be positive or negative. *Figure 1* illustrates the simplified schematic of a Triac or an ACST and the associated silicon structure. A Triac or an ACST could be switched on by a positive or a negative gate current through the diodes embedded back-to-back between G and A1. These 2 diodes are implemented at the P1-N1 and P1-N2 junctions.

Figure 1. Simplified schematic and silicon structure of Triac / ACST circuit



The silicon structure of an ACS is different from a Triac or an ACST (see *Figure 2*). Here the gate is the emitter of a NPN bipolar transistor. So there is only one PN junction implemented by P1 and N1. The gate current can then only be sunk from the gate, and not sourced to it.

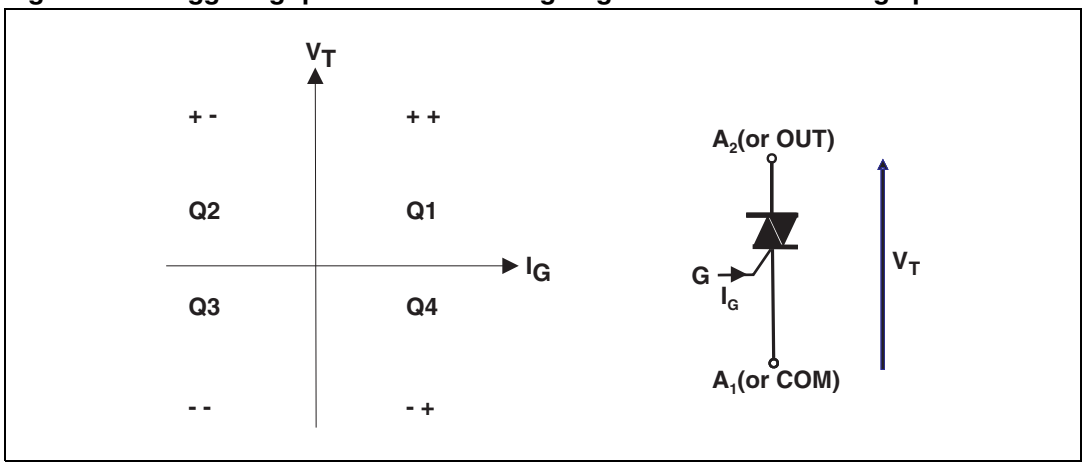
Figure 2. Simplified schematic and silicon structure of an ACS



Four triggering quadrants can be defined according to the polarity of the gate current and the polarity of the voltage applied across the device, as shown on *Figure 3.*

For an SCR, only a positive gate current can switch-on the device. Thus, the triggering quadrants are not considered for SCR devices.

Figure 3. Triggering quadrants according to gate current and voltage polarities



The usable triggering quadrants depend on the family and the class of the device used. *Table 1* shows the triggering quadrants available for ST Microelectronics devices.

Table 1. Available triggering quadrants according to device family and class

Family	Class	Triggering quadrants			
		Q1	Q2	Q3	Q4
Triac	Standard	Yes	Yes	Yes	Yes
	Snubberless and logic level	Yes	Yes	Yes	No
	Snubberless high temperature	Yes	Yes	Yes	No
ACS / ACST	ACS	No	Yes	Yes	No
	ACST	Yes	Yes	Yes	No

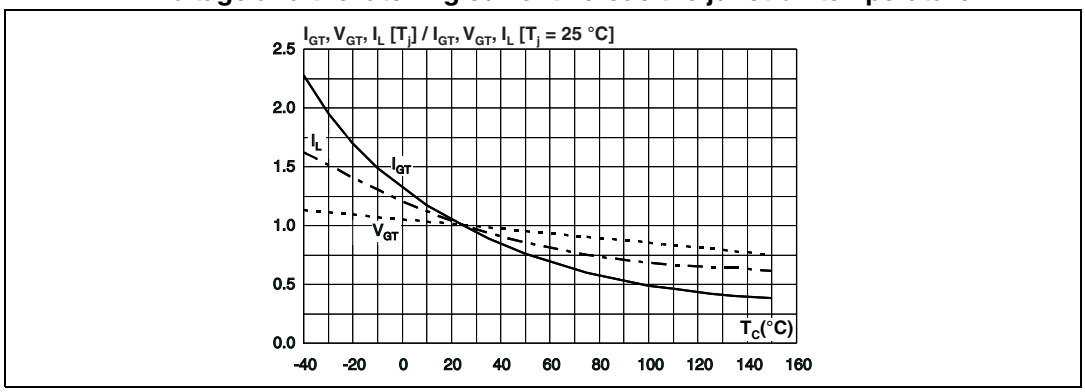
As the triggering quadrants Q2 and Q3 are common to all Triacs and ACS / ACST devices, the control mode in Q2 and Q3 is recommended. In this way the replacement of one device by another one (for example, if an ACST is used in place of a standard Triac) is possible. Triggering in Q4 is not advised because the triggering gate current is the highest. Also the dI/dt capability of Triacs is lower in Q4 compared to the other quadrants. Working in Q2 / Q3 quadrants is then advised, even for standard Triacs, to decrease the board consumption and increase the board reliability.

To design the control circuit and the power supply, the device triggering parameters must be considered, i.e. the triggering gate current I_{GT}, the triggering gate voltage V_{GT} and the latching current I_L.

- I_{GT} is the minimum gate current to turn on the device. This current has to be applied between gate and cathode for an SCR, gate and A1 for a Triac or gate and COM for an ACS / ACST. The applied gate current must be higher than the I_{GT} specified at the lowest expected operating temperature. As a high gate current value provides an efficient triggering, a gate current of twice the specified I_{GT} is recommended.
- V_{GT} is the voltage measured between gate and cathode for an SCR, gate and A1 for a Triac or gate and COM for an ACS / ACST when the I_{GT} current is applied.
- I_L is the latching current. The latching current is the minimum value that the load current must reach before gate current removal to avoid device switch-off (see Reference *1*).

These parameters are specified at 25 °C and vary with the junction temperature as shown in *Figure 4.* The I_{GT}, V_{GT} and I_L variations are the same for most devices, except for sensitive and low current SCRs (P0102BL, P01, X06, X02, X04 and TS420 series) and for ACS / ACST devices.

Figure 4. Typical variations of the triggering gate current, the triggering gate voltage and the latching current versus the junction temperature



2 Triggering circuits

2.1 Two kind of power supply bias

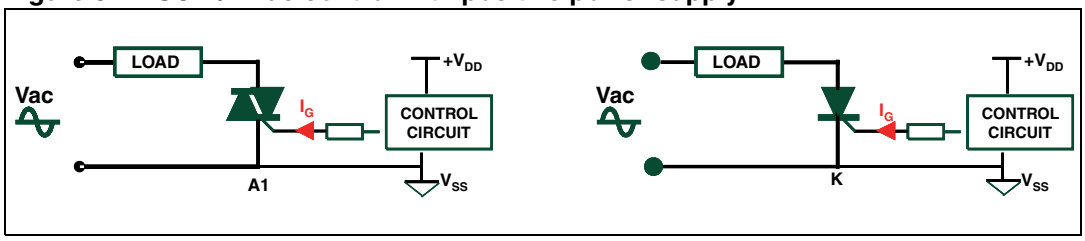
To trigger a Triac, ACST, ACS or SCR, a gate current has to be applied on the gate pin and circulates between gate and cathode (K) for SCR, or between gate and terminal A1 for Triac, or between gate and terminal COM for ACST and ACS.

For non-insulated control circuits, this means that the reference of the control circuit has to be related to K, A1 or COM. Then there are two ways to connect this drive reference.

- Solution 1: connect the control circuit ground (V_{SS}) to K or A1
- Solution 2: connect the control circuit voltage supply (V_{DD}) to A1 or COM

Solution 1 is called a positive power supply. The voltage supply V_{DD} is indeed above the drive reference (V_{SS}) which is connected to the mains terminal (line or neutral) as shown in *Figure 5.* If the supply is a 5 V power supply, then V_{DD} is 5 V above the mains reference.

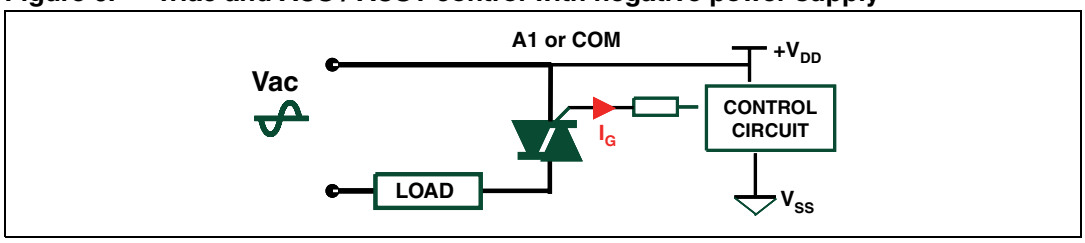
Figure 5. SCR / Triac control with positive power supply



Solution 2 is called a negative power supply. The voltage supply reference (V_{SS}) is indeed below A1 or COM, which is connected to the mains reference (line or neutral) as shown in *Figure 6.* If the supply is a 5 V power supply, then V_{SS} is 5 V below the line reference.

This topology can be used with all Triacs, ACS and ACST, but not with SCR.

Figure 6. Triac and ACS / ACST control with negative power supply



2.2 Gate resistor value definition

The minimum gate current (I_{GT}) required to trigger a Triac, SCR or ACS / ACST increases as the junction temperature (T_j) decreases (see *Figure 4*). The worst case appears when T_j equals the minimum ambient temperature. For appliance systems, the minimum ambient temperature is generally 0 °C.

For example, the ACS108-6Tx I_{GT} level is given as lower than 10 mA with T_j equals 25 °C. When T_j equals 0 °C, I_{GT} becomes 15 mA.

In the following, we assume that the device gate is directly connected to a microcontroller (MCU) output pin, through a gate resistor (R_G).

To ensure that the MCU will always deliver "I_{GT}(0 °C)", the maximum gate current at 0 °C, the value of the gate resistor (R_G) must be calculated for the minimum available voltage. This means that the minimum supply voltage and the maximum voltage drop of the gate junction (V_{GT}) should be taken into account.

The actual resistance value also depends on its tolerance. Typically, 1% precision resistors are used. The microcontroller output port resistor (R_{DSon}) maximum value also plays a role in the current limitation.

The required value of R_G is given in *Equation 1*.

Equation 1

$$\frac{V_{DD\,min} - V_{GT\,max}}{R_{DSon\,max} + R_G \cdot 1{,}01} > I_{gt}(0\,°C)$$

Example: for a 20 mA output pin of a microcontroller, the worst R_{DSon} could equal typically 50 Ω (ex: 1.5 V for 30 mA for an 85 °C junction temperature).

If an ACST6 is used, its I_{GT} increases by 35% for a 0 °C junction temperature, compared to the 10 mA given at 25 °C. V_{GT} is given for T_j equals 25 °C. Its value increases as T_j decreases with a 2 mV/ °C rate. With a minimum supply voltage of 4.5 V and V_{GT} equals 1.55 V (at 0 °C), R_G is given in *Equation 2* for ACST6 devices.

Equation 2

$$R_g < \frac{4{,}5 - 1{,}55}{0{,}0135 \cdot 1{,}01} - 50 \quad = \quad 166\ \Omega$$

The normalized value closest to 166 Ω is 165 Ω (1% precision resistor).

2.3 SCR and Triac triggering circuit with a positive power supply

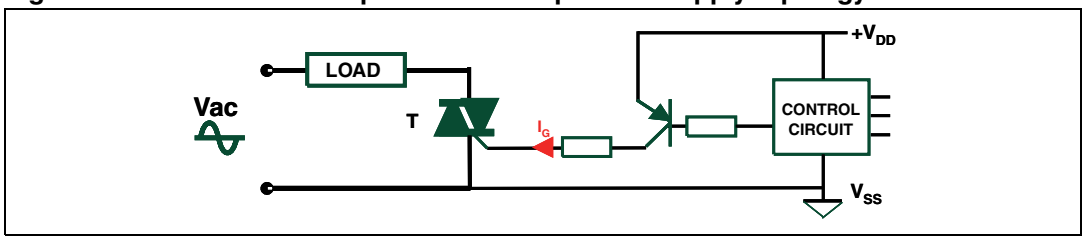
With positive power supplies, the gate current can be only sourced from the control circuit to the gate. Such a topology is adapted for SCRs control. For Triacs, the devices are then triggered in quadrants Q1 and Q4. Such an operation is not advised for Triacs as the gate current level is the highest for Q4 (see *Section 1*). Also Triac resistance to dI/dt at turn on is lower for Q4.

As a control circuit designed with a positive power supply can be used only with standard Triacs, the whole design has to be changed if the designer wants to switch from this standard Triac to a snubberless or logic level Triac, or to an ACS or ACST. Indeed these latter devices can not be triggered in Q4 (refer to *Section 1*).

When the gate current required to trigger the device is higher than the control-circuit output current capability, the control-circuit output current has to be amplified. For example, today a lot of MCUs feature output pins with a current capability around 30 mA. They can switch Triacs safely with I_{GT} up to 15 to 20 mA. If a Triac with a 35 or 50 mA I_{GT} has to be controlled by such an MCU, the two solutions are then:

- Use several MCU output pins in parallel (the best is to use a separate gate resistor between each output pin and the Triac gate to ensure a good current repartition between each pin).
- Use a bipolar transistor as shown in *Figure 7.*

Figure 7. Gate current amplification with positive supply topology



With the bipolar solution, to keep the current sourced to the gate, the only way is then to use a PNP transistor. A PNP transistor has to be used to set its drive reference to a stable bias, which is the power supply (V_{DD}) in this case.

This is another drawback of the positive power supply topology. To amplify the control circuit output current, a PNP transistor has to be used instead of an NPN transistor. And a PNP transistor has a lower current gain and a higher price than an NPN one.

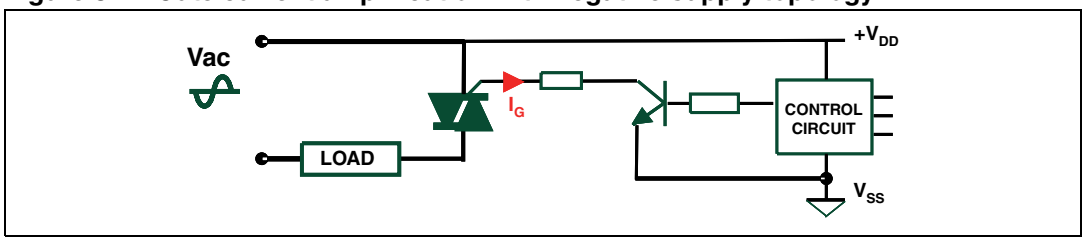
2.4 Triac and ACS / ACST triggering circuit with negative power supply

Such a topology is the preferred one. The gate current is sunk from the gate by the control circuit. The device then works in Q2 and Q3 quadrants. Such a topology is adapted for all devices: standard, snubberless or logic level Triacs, and ACS or ACST.

For SCRs, the gate circuit has to be modified to source the current to the gate, as explained in *Section 2.5*.

It should be noted that another advantage with this topology is that the control circuit output current can be easily amplified if needed (see *Section 2.3*) with an NPN transistor as shown in *Figure 8.*

Figure 8. Gate current amplification with negative supply topology



2.5 SCR triggering circuit with negative power supply

In the previous section, it has been demonstrated that choosing a negative power supply is the best solution to control Triac or ACS / ACST. But in some applications, an electronic circuit may have to control both Triac and SCR. And SCR can only be triggered by sourcing a current to the gate.

Such applications are encountered when a switch has to control a DC load on the mains. This occurs for example for some pumps used in coffee machines, which feature an internal diode (see *Figure 9*). Also some magnetic door locks can be controlled only during one half cycle. Then an SCR can be a cheaper solution than a Triac.

The circuit has then to be modified to allow the SCR to be triggered from a negative power supply. The schematic in *Figure 9* shows the addition of a PNP transistor (Q1), a low-voltage diode (D1), a resistor (R2) and a capacitor (C1). This schematic is similar to the schematic used to trigger Triacs with a positive power supply [see Reference *2*].

The circuit operation is the following:

1. Q1 is OFF, C1 capacitor is charged thanks to D1 and R3.
2. Q1 is switched on by the “CTRL” signal, C1 capacitor is discharged through R2, the SCR gate and Q1. A positive gate current pulse is then applied and the SCR switches on.

C2 capacitor is used to increase the dV/dt immunity of X1 SCR, which is a very sensitive device (I_{GT} < 200 µA for X00602 devices).

The gate pulse width has to be set by the values of R2 and C1. The point is to keep the gate current above max. I_{GT} up to the moment the anode current (I_T) is above the maximum latching current. For example, for the X00602, I_L can reach up to 7 mA for a -20 °C junction temperature.

With the load used in this application, a gate current pulse width longer than 200 µs (t_p) is required to reach 7 mA on I_T. With the component values given in *Figure 9*, X1 gate current remains above 2.4 mA during the whole “CTRL” pulse which lasts 400 µs (see *Figure 10*). This allows correct operation even for very low ambient temperature operation.

Note: As gate current is very low, it can be estimated using the value of V_D (see Figure 10), $I_G \approx (V_D - 0.6\ V) / R2$

Figure 9. Drive schematic to trigger an SCR with a negative power supply

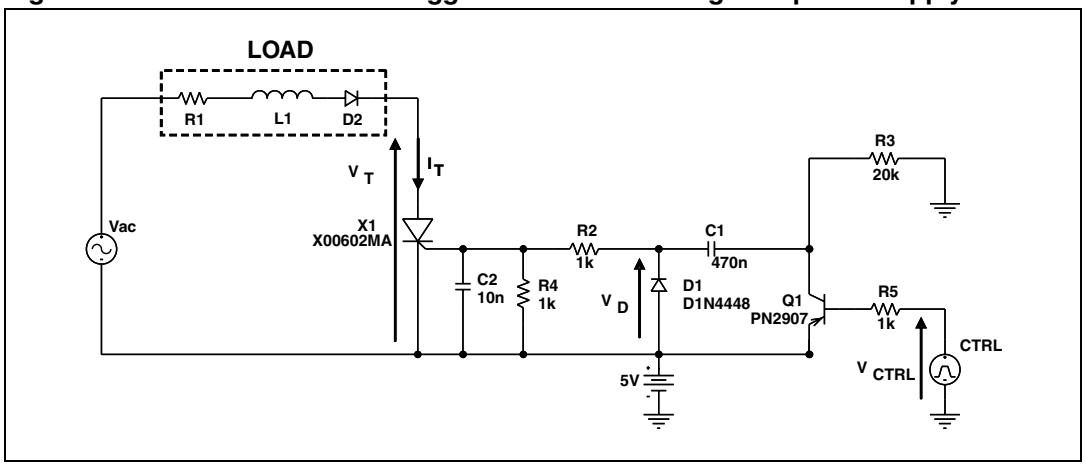
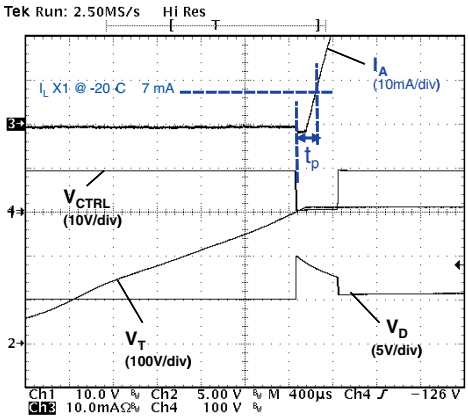


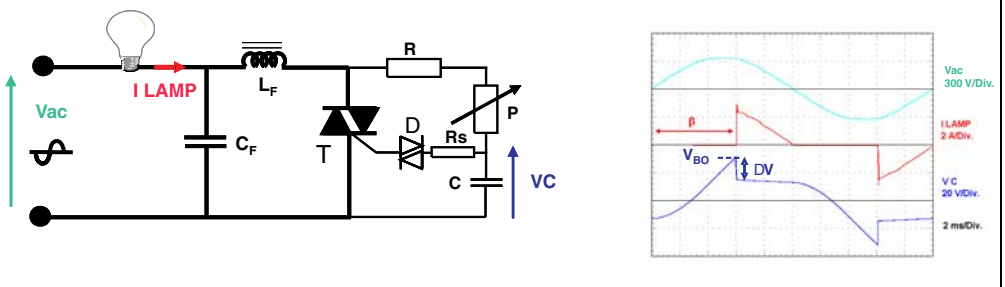
Figure 10. Experimental validation of SCR triggering



2.6 Diac control circuit

A Diac-based circuit can be used for non-insulated control circuits. Such a circuit is very simple and known since the 70's. It was traditionally used for light dimmers or universal motor speed-control circuits. *Figure 11* gives the typical schematic for a light dimmer. L_F and C_F are respectively the filter inductor and capacitor used to reduce the conducted electromagnetic noise coming from Triac switch-on at voltage levels different from zero. The circuit will be similar for a universal motor speed control circuit. The filter is then placed before mains input as the noise comes mainly from motor brush commutations.

Figure 11. Diac-based light dimmer



The operation of the dimmer circuit shown on *Figure 11* is as follows:

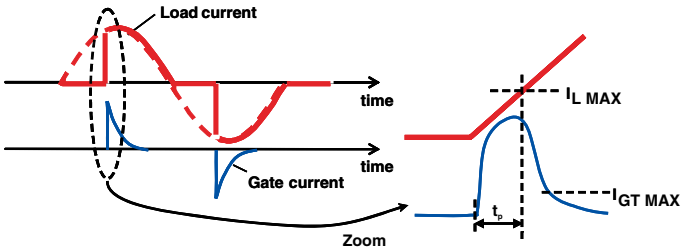
1. The capacitor C is charged through the resistive potentiometer (P)
2. When V_C reaches the Diac breakover voltage (V_{BO}), the Diac turns on and its voltage is decreased by ΔV. Capacitor C is also discharged (ΔV reduction), this results in a discharge current which is applied to the Triac gate. Rs is used to enlarge the gate current pulse width. T is then switched on. Here, for the positive line polarity, T is triggered in Q1.
3. T remains on until the next zero current crossing point. As T is on, there is no more high voltage applied between A1 and A2, and the Diac is not charged anymore

4. T Triac switches off when its current reaches zero. Then the mains voltage is applied back between A1 and A2. So Capacitor C is then recharged in negative bias. This will go on until the negative diac V_{BO} is reached.
5. Triac T is switched on as explained on point 2 but here in Q3 (current sunk from the gate and negative V_{A2-A1} voltage).

This means that ACS can not be triggered by such circuits as they need that their gate current is always sunk from the gate (i.e. only Q2 and Q3 triggering is possible).

The main point to check with Diac-based circuits is that the gate current pulse width lasts enough time to allow the Triac anode current to reach the latching level I_L (see Reference *1* for further information on this parameter). *Figure 12* explains this point. The gate current has to be higher than the maximum specified I_{GT} up to reaching a load current, i.e an anode current, higher than the maximum latching current (according to datasheet maximum value, but also for the lowest junction temperature as I_L increases with temperature decrease). This will ensure a correct Triac turn on.

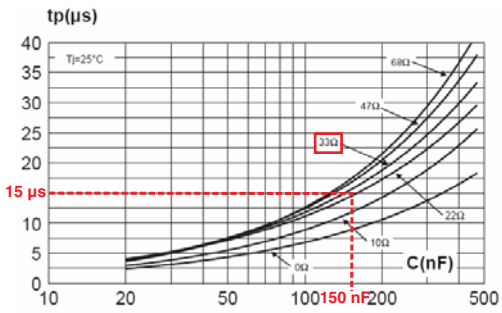
Figure 12. Required gate pulse width, with Diac circuit, to trigger the Triac



When the pulse width (t_p) is defined, *Figure 13* (from the DB3TG datasheet) can then be used to define the Rs and C values. For example, if a 15 µs pulse width is required, a 33 Ω resistor Rs is required with a 150 nF capacitor C.

It should be noted also that resistor Rs is helpful to keep Diac current below its maximum repetitive current allowed (I_{TRM} parameter).

Figure 13. Typical pulse width duration versus Rs and C values

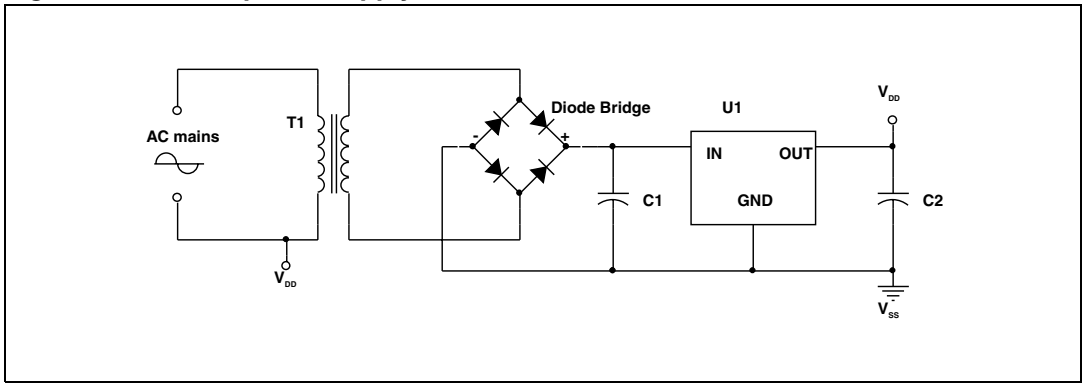


3 Examples of negative power supplies

3.1 Linear power supply

The linear power supply is composed of a step down transformer, a diode bridge, a linear regulator (U1) and some filtering capacitors (see *Figure 14*).

Figure 14. Linear power supply



The output current (I_{DC}) depends on the power of the transformer (S), the output voltage (V_{DC}) and the power factor (pf) of such a power supply. Due to the high mains current harmonic content, a 0.5 power factor can usually be assumed. Without consideration of the transformer, diodes and regulator power losses, the output current is then in *Equation 3*.

Equation 3

$$I_{DC} = \frac{S \times pf}{V_{DC}}$$

For a typical power factor of 0.5 and a 230 V / 15 V step down transformer, the calculated output current capability and the measured typical standby power consumption (P_{OFF}) are given according to the transformer power on *Table 2.*

Table 2. Calculated output DC current and measured typical standby power consumption

Transformer power, S	1.6 VA	3 VA	10 VA
Output DC current, I_{DC}	53 mA	100 mA	333 mA
Stand-by power consumption, P_{OFF} (measured)	0.08 W	0.5 W	1.1 W

The benefits of this solution are:

- High output current
- Possibility to easily generate multiple output voltages by using several secondary windings

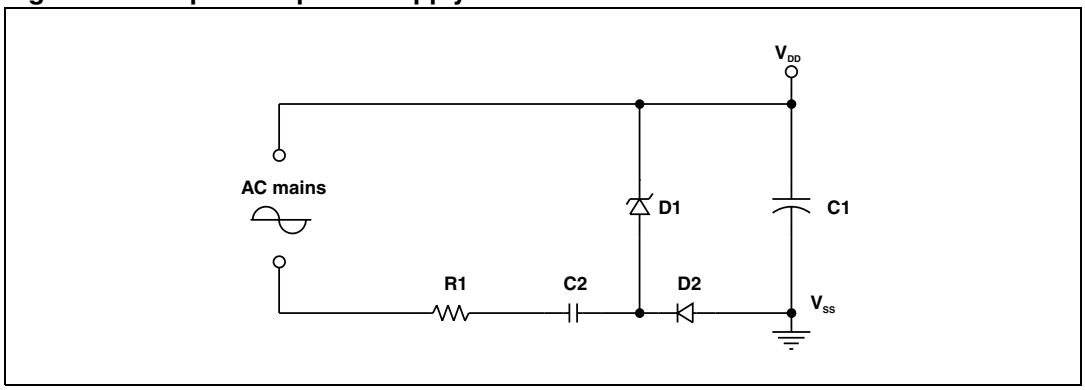
The drawbacks of this solution are:

- High cost
- High standby losses (due to the transformer magnetizing current)
- Bulky size of the 50 Hz transformer

3.2 Capacitive power supply

Figure 15 shows the schematic diagram of a capacitive negative power supply.

Figure 15. Capacitive power supply



To have a constant voltage across C1, the average value of the input current ($I_{IN(av)}$) must be equal to the average value of the output current ($I_{OUT(av)}$). The input current is a half-wave rectified current, whose average value ($I_{IN(av)}$) is given in *Equation 4* (R1 and C1 impedances and diode D2 voltage drop are neglected):

Equation 4

$$I_{IN(av)} = 2 \times f \times C2 \times V_{mains(peak)} = I_{OUT(av)}$$

The standby power consumption (P_{OFF}) is set by the R1 resistor value, the average input current and the D1 zener voltage (V_Z). The resistor R1 is required to limit the inrush current stress at power supply turn on and to avoid the overrating of the current protection of the circuit. The standby power consumption is:

Equation 5

$$P_{OFF} = R1 \times (I_{IN(av)} \times \frac{\pi}{\sqrt{2}})^2 + V_Z \times I_{IN(av)}$$

For a 230 V / 50 Hz mains voltage, a 60 Ω resistor R1 (typical value) and a 15 V zener diode, the calculated average output current and standby power consumption versus different AC capacitors given in *Table 3*.

Table 3. Calculated output DC current and measured typical standby power consumption

AC capacitor, C2	220 nF	470 nF	680 nF	1 µF
Average output DC current, $I_{OUT(av)}$	7.1 mA	15.3 mA	22.1 mA	32.5 mA
Stand-by power consumption, P_{OFF}	0.12 W	0.3 W	0.48 W	0.8 W

The benefits of this solution are:

- Low cost (for output current lower than 20 mA)
- Small size
- Easy to implement

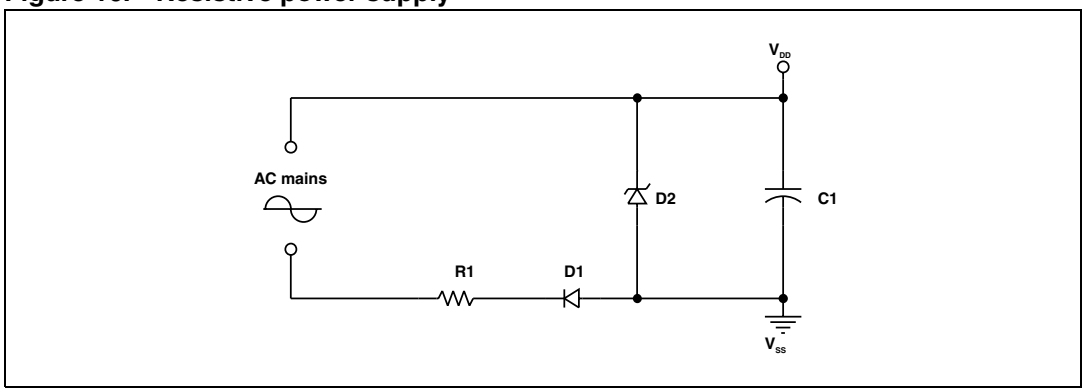
The drawbacks of this solution are:

- Low average output current. The maximum average output current is about 30 mA. For higher output current, the size and the cost of the C2 capacitor becomes prohibitive. Moreover, the inrush current stress at power supply turn on increases and will need higher resistor R1 power.
- High standby power consumption. For example, the standby power consumption equals about 0.8 W for a 230 V power supply with a capacitor C2 of 1 µF, a 15 V zener diode and a 60 Ω R1.

3.3 Resistive power supply

Figure 16 show the schematic diagram of a negative resistive power supply.

Figure 16. Resistive power supply



To have a constant voltage across C1, the average value of the input current ($I_{IN(av)}$) must be equal to the average value of the output current ($I_{OUT(av)}$). The input current is a half-wave rectified current, whose average value is given by the following equation (C1 impedance and diode D1 voltage drop neglected):

Equation 6

$$I_{IN(av)} = \frac{V_{mains(peak)} - V_z}{R1 \times \pi} = I_{OUT(av)}$$

The standby power consumption (P_{OFF}) is set by the R1 resistor value and is equal to:

Equation 7

$$P_{OFF} = \frac{(V_{mains(peak)} - V_z)^2}{4 \times R1}$$

For a 230 V mains voltage and a 15 V zener voltage, the calculated average output current and standby power consumption versus different resistors are:

Table 4. Calculated average output DC current and standby power consumption

Resistor R1	25 kΩ	18 kΩ	12 kΩ	8 kΩ
Average output DC current, $I_{OUT(av)}$	3.9 mA	5.5 mA	8.2 mA	12.3 mA
Stand-by power consumption, P_{OFF}	1 W	1.3 W	2 W	3 W

The benefits of this solution are:

- Low cost (for output currents < 10 mA)
- Small size
- Easy to implement

The drawbacks of this solution are:

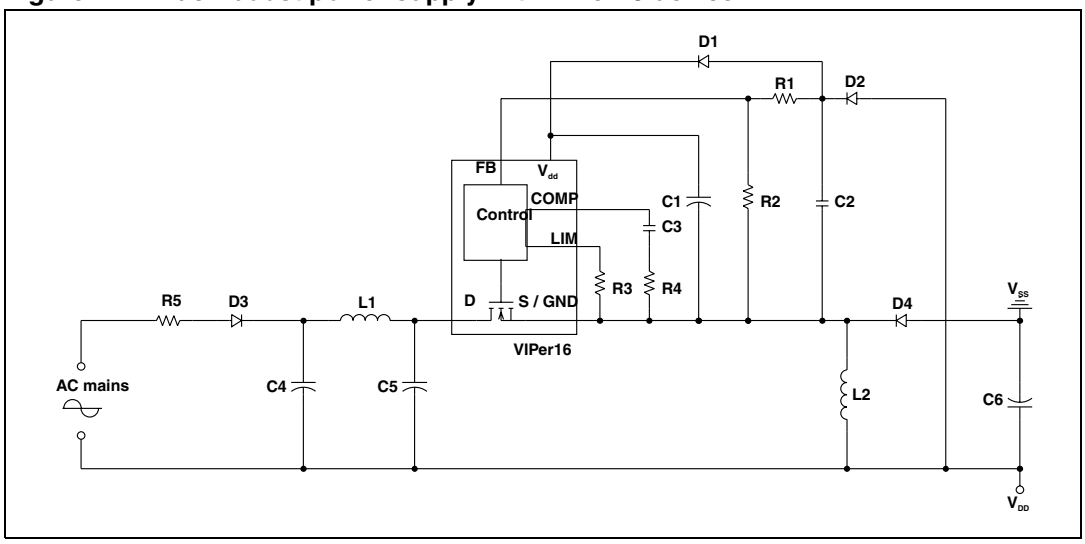
- High resistor power dissipation. The resistor value is typically limited to 8 kΩ in order to limit its power dissipation to 3 W.
- Low average output current. The maximum average output current for such supplies is about 12 mA. For higher output current, the cost and the power dissipated by R1 becomes prohibitive.
- Stand-by power consumption. For an 8 kΩ resistor, a 15 V zener diode and 230 V mains voltage, the standby power consumption is about 3 W.

3.4 Buck-boost power supply

The first example of switched mode power supplies (SMPS) that can be used to convert AC mains voltage to DC voltage is the buck-boost converter. The buck-boost converter is the simplest converter to implement a negative power supply. It should be noted that only positive power supply can be implemented with a buck converter.

Figure 17 show the schematic diagram of a buck-boost negative power supply using VIPer16 device.

Figure 17. Buck-boost power supply with VIPer16 device



When the VIPer MOSFET is on, the energy is stored in the inductance L2. When the VIPer MOSFET is switched off, the energy stored during on time is supplied to the output capacitor C6.

The input voltage is a half-wave rectified and filtered signal from diode D3 and filter PI (C4, C5 and L1). The input voltage is close to the peak mains voltage, so close to 325 V for a 230 V mains. As the input voltage is much higher than the output voltage (typically 3.3 V, 5 V or 15 V), the switching duty cycle is very low (few %). Thanks to the VIPer integrated regulator, a low duty cycle does not significantly affect operation. The buck-boost converter typically

operates in discontinuous mode. Discontinuous mode has the advantage of reducing the size and the cost of the inductance with respect to continuous mode.

Equation 8 gives a simplified relation between the average output DC current and the inductance value for discontinuous mode (VIPer power losses not considered).

Equation 8

$$I_{OUT} = \frac{\alpha^2 \times V_{mains(peak)}^{\ 2}}{2 \times L2 \times f \times V_{OUT}}$$

The minimum inductance value is limited by the VIPer peak current limitation (I_{Dlim}). For VIPer16 device, the typical peak current limitation is 400 mA. The minimum inductance in discontinuous mode is given by:

Equation 9

$$L2_{(min)} = \frac{V_{mains(peak)} \times \alpha}{I_{Dlim} \times f}$$

The ratio between output and input voltages is used to define the VIPer duty cycle.

Equation 10

$$\frac{V_s}{V_e} = \frac{\alpha}{1-\alpha} \quad \text{so} \quad \alpha = \frac{V_s}{V_s + V_e}$$

For a 230 V mains voltage, a 12 V output voltage and a 60 kHz switching frequency (VIPer16 typical frequency), the average output current versus different inductances and the typical standby power consumption are:

Table 5. Calculated average output DC current (≈ 0.035) and typical standby losses

L2 inductance	900 µH	800 µH	700 µH	600 µH (min. value)
Average output DC current, $I_{OUT(av)}$	100 mA	115 mA	130 mA	155 mA
Stand-by power consumption, P_{OFF}	≈ 100 mW			

The advantage of a buck-boost converter compared to a buck converter is that there is no need for an added output load resistance or output Zener (see Reference *3*). For both topologies, the feedback capacitor is still discharged with the IC feedback pin current, whereas the output capacitor is not discharged if the output current is zero. The feedback capacitor then indicates a lower output level than reality. Furthermore, this drawback is amplified by the buck topology as the output capacitor is charged during each MOSFET on time, whereas the feedback capacitor is not. So output voltage can increase to an excessive value and has to be clamped.

The added resistance or clamping diode is then required at the buck output to avoid an excessive output voltage in case of no-load or very light load.

With a buck-boost converter, the output capacitor is not charged during MOSFET on time. Furthermore, the output voltage capacitor (C6) can not be charged if the feedback capacitor (C2) voltage is lower than C6, as diode D2 is blocked. So there is no risk of an excessive output voltage and the clamping device is not required.

For a buck-boost converter the efficiency (as well as the maximum output current) should be lower and the output capacitor bigger than for a buck converter, as the whole inductor current is used to charge the output capacitor for the buck converter. But for 230 V AC / 12 V DC, the duty cycle is very low so there is no great difference between buck and buck-boost performances. Similar efficiency is reached for both topologies, with the same reactive components.

3.5 Flyback power supply

The second SMPS topology widely used today by designers is the flyback topology. This converter uses a transformer to store the energy instead of an inductance. The benefit of this solution, compared to a buck-boost converter, is the possibility to insulate the output voltage and also to generate several output voltages by using several secondary windings. A flyback converter can also deliver a higher power with the same monolithic device (VIPer) compared to a buck or buck-boost converter.

For AC switch control, as the V_{DD} level has to be connected to the mains, there is no interest in implementing an insulated power supply. So only the advantage of implementing a 2nd low-voltage supply will push designers to use such a topology. Note that this 2nd supply can then be insulated from the mains.

It is easy to implement a negative supply with a flyback converter, and the output voltage is insulated from the mains. So the V_{DD} terminal can either be connected to the neutral or the line. The V_{DD} voltage is then no longer insulated from the mains. This means that the insulation has to be implemented elsewhere to protect the appliance user from electrical shocks (for example, with an insulated keyboard and display).

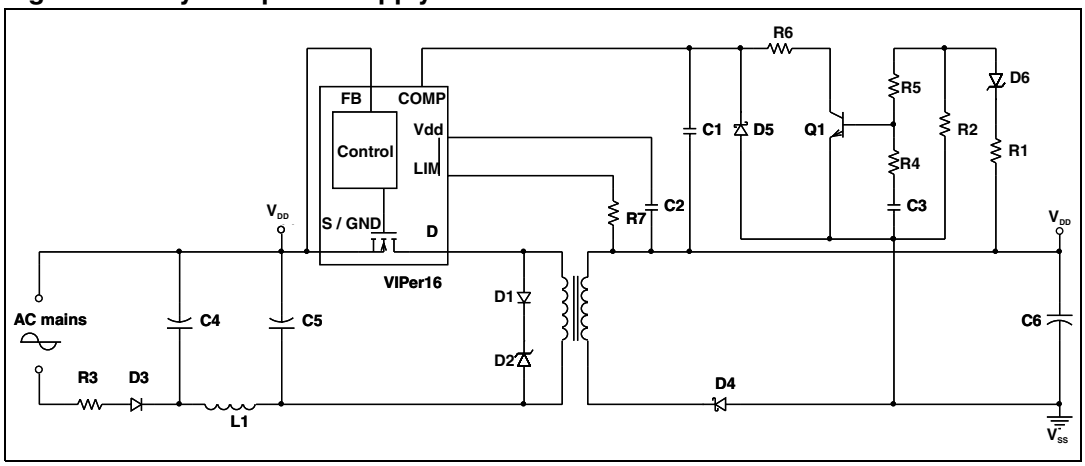
Note also that due to the transformer ratio, a flyback converter can work with a higher duty cycle than a buck-boost converter. The input peak current is then lower with a flyback converter than with a buck-boost converter. The MOSFET peak current is thus lower and so are its switching losses. The flyback converter efficiency can then be slightly better.

As for buck-boost converter, the VIPer operates in discontinuous mode.

The drawback of the flyback solution is that the transformer used most of the time is a specific device, whereas a standard inductance can be used with a buck-boost converter. Consequently, the flyback converter cost could be higher by about 15% than the buck-boost converter cost for the same output power.

Figure 18 shows the schematic diagram of a flyback power supply using a VIPer16 device. For a 230 V mains voltage and a 5 V output voltage, the standby power consumption is typically around 70 mW with this circuit.

Figure 18. Flyback power supply with VIPer16 device



For flyback converter design, please refer to the technical note TN0023 from STMicroelectronics.

3.6 Comparison of negative power supplies

Table 6 summarizes the advantages and drawbacks of the negative power supplies introduced in the point 3 according to the cost, the size, the easiness of implementation, the standby power consumption, the output current capability and the capability to generate easily one or more output voltages.

Table 6. Comparison of negative power supplies(1)

Power supply type	Cost	Size	Easy of implementation	Standby power consumption	Output	
					Max. current level	Number
Linear	-	--	++	--	+	1 or more
Capacitive	+	-	++	-	--	1
Resistive	-	+	++	--	---	1
Buck-boost	++	++	+	+++	+++	1
Flyback	+	+	+	+++	++++	1 or more

1. Key: +: good, -: bad

4 Conclusion

This application note has presented circuits that can be used to control SCR, Triacs or ACS / ACST devices, as far as a non-insulated circuit is allowed.

It has been shown that a negative power supply is the best topology as it can be used for all AC switches. Moreover if an SCR has to be controlled with a board using a negative supply to trigger AC switches, a simple schematic has been presented to control the SCR with the same supply.

Schematics for negative switched mode power supplies have been presented.

Even if the first reflex of a designer is to implement a positive power supply, negative power supplies are as easy to implement as positive ones. There are also some benefits with a negative supply topology such as, for example, the removal of output overvoltage protection for non-insulated SMPS (buck-boost topology compared to buck topology), optotransistor removal (for flyback converters) and the use of NPN transistors instead of PNP to amplify the gate current.

5 References

1. “Latching current”, Application note AN303, STMicroelectronics.
2. “QII and QIII Triac triggering with positive power supply”, Application note AN440, STMicroelectronics.
3. “VIPower: Low Cost Power Supplies Using VIPer12A in Non Isolated Applications”, N. Aiello - F. Gennaro - R. Santori, Application note AN1357, STMicroelectronics, 2001.
4. “Discontinuous Flyback transformer description and design parameters”, Technical note TN0023, STMicroelectronics.

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
09-Mar-2010	1	Initial release.